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10/524,458	02/10/2005	Thomas Franciscus Waayers	NL02 0749 US	6330

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EXAMINER	
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ART UNIT	PAPER NUMBER
2863	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/524,458	WAAYERS, THOMAS FRANCISCUS	
	Examiner	Art Unit	
	TOAN M. LE	2863	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 October 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *13-16* is/are allowed.

6)☒ Claim(s) *1-3,11 and 12* is/are rejected.

7)☒ Claim(s) *4-10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 February 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-3 and 11-12 are rejected under 35 U.S.C. 102(e) as being anticipated by Jacobson (US Patent No. 6,499,124).

Referring to claim 1, Jacobson discloses a module comprising a functional block and a test controller for controlling the functional block in an evaluation mode of the module, the test controller comprising:

a plurality of pins including an input pin "TDI" of the input/output (IOB) (Figures 6(A), 6(B), 6(C), 8, 10-13)and an output pin "TDO" of the input/output (IOB) (Figures 6(A), 6(B), 6(C), 8, 10-13);

a first register "601(1)" (Figure 8: register 601(1) having update register "630(1)", shift register "610(1)") coupled between the input pin "TDI" and the output pin "TDO" for receiving a bit pattern via the input pin "TDI" and outputting the bit pattern via the output pin "TDO"(col. 7, lines 59-67 to col. 8, lines 1-31; col. 10, lines 39-67 to col. 11, lines 1-14); and

a second register "601(2)" (Figure 8: register 601(2) having update register "630(2)", shift register "610(2)") coupled to the first register for capturing the bit pattern responsive to an update signal (col. 7, lines 59-67 to col. 8, lines 1-31; col. 10, lines 39-67 to col. 11, lines 1-14);

characterized in that the test controller further comprises dedicated control circuitry 650-A(1)/650-A(2)/650-A(3) ("Security Circuit" in Figure 8) for blocking the update signal responsive to the bit pattern (col. 6, lines 32-67 to col. 7, lines 1-4; col. 8, lines 32-59; col. 9, lines 15-61; col. 10, lines 39-67 to col. 11, lines 1-32 and lines 51-67 to col. 12, lines 1-3).

As to claim 2, Jacobson discloses a module comprising a functional block and a test controller for controlling the functional block in an evaluation mode of the module, characterized in that the dedicated control circuitry comprises a first logic gate having:

a first input for receiving the update signal "676" from memory "660" (Figure 6(A));

a second input "672" (Figure 6(A) coupled to the first register 601(1) for receiving the bit pattern; and

an output "674" (Figure 6(A)) coupled to the second register 601(2) (col. 8, lines 32-59).

Referring to claim 3, Jacobson discloses a module comprising a functional block and a test controller for controlling the functional block in an evaluation mode of the module, characterized in that the dedicated control circuitry further comprises a plurality of logic gates "Switch" (Figure 6(A))coupled between the first register and the second input of the first logic gate for providing the second input with the bit pattern in a modified form (col. 8, lines 32-59).

As to claim 11, Jacobson discloses an electronic device comprising a plurality of modules being substantially serially interconnected in an evaluation mode through respective input pins and output pins, a module from the plurality of interconnected modules comprising a functional block and a test controller for controlling the functional block in the evaluation mode of the module, the test controller comprising:

a plurality of pins including an input pin from the respective input pins ("TDI" of the input/output (IOB) (Figures 6(A)) and an output pin from the respective output pins "TDO" of the input/output (IOB) (Figures 6(A), 6(B), 6(C), 8, 10-13);

a first register "601(1)" (Figure 8: register 601(1) having update register "630(1)", shift register "610(1)") coupled between the input pin "TDI" and the output pin "TDO" and the output pin for receiving a bit pattern via the input pin and outputting the bit pattern via the output pin "TDO" (col. 7, lines 59-67 to col. 8, lines 1-31; col. 10, lines 39-67 to col. 11, lines 1-14); and

a second register "601(2)" (Figure 8: register 601(2) having update register "630(2)", shift register "610(2)") coupled to the first register for capturing the bit pattern responsive to an update signal (col. 7, lines 59-67 to col. 8, lines 1-31; col. 10, lines 39-67 to col. 11, lines 1-14);

characterized in that the test controller further comprises dedicated control circuitry 650-A(1)/650-A(2)/650-A(3) ("Security Circuit" in Figure 8) for blocking the update signal responsive to the bit pattern (col. 6, lines 32-67 to col. 7, lines 1-4; col. 8, lines 32-59; col. 9, lines 15-61; col. 10, lines 39-67 to col. 11, lines 1-32; col. 10, lines 39-67 to col. 11, lines 1-32 and lines 51-67 to col. 12, lines 1-3).

Referring to claim 12, Jacobson discloses an evaluation tool comprising a set of bit patterns for evaluating an electronic device as claimed in claim 11 by providing the electronic device with the set of bit patterns, characterized in that the set of bit patterns comprises a bit pattern for triggering the control circuitry to block the update signal responsive to the bit pattern (col. 6, lines 32-67 to col. 7, lines 1-4; col. 8, lines 32-59; col. 9, lines 15-61).

Allowable Subject Matter

Claims 4-10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The reason for allowance of claim 4 is the inclusion of a no-updated bypass register coupled between the input pin and the second input of the multiplexer.

The reason for allowance of claims 5-6 is they depend on allowable claim 4.

The reason for allowance of claim 7 is the inclusion of a further multiplexer, a first further register, a second further register, and a conductor coupled between the input pin and the second input of the further multiplexer.

The reason for allowance of claims 8-10 is they depend on allowable claim 7.

Allowable Subject Matter

Claims 13-14 are allowed.

The reason for allowance of claim 13 is the inclusion of a no-updated bypass register coupled between the input pin and the second input of the multiplexer.

Response to Arguments

Applicant's arguments filed 10/2/08 have been fully considered but they are not persuasive.

Referring to claim 1, Applicant argues:

"Referring to limitations of independent claim 1 (and as relevant to limitations of independent claim 11), the Office Action has asserted that the '124 reference discloses a 'first register,' 'second register' and 'dedicated control circuitry' as claimed. However, the cited security circuit 650-A(1) in FIG. 8 of the '124 reference, which Office Action has alleged as

providing correspondence to the claimed 'dedicated control circuitry,' does not block any update signal and does not operate in response to a bit pattern captured by a second register as claimed. Referring to FIG. 8, the cited security circuit 650-A(1) is coupled to a node between a shift register flip-flop 620(1) and a parallel latch 630 (1), via conductive segment 625(1). The security circuit 650-A(1) functions to either pass or block a test data out (TDO) signal from passing between BSR cells in response to a stored security code, where the passage of TDO signals between the BSR cells is not dependent upon any update signal (see, e.g., columns 8:66-9:14 and column 10:58-64). The cited 'updated' signal in the cited '124 reference is provided from a TAP controller to the parallel latch 630, independently from the security circuit 650-A(1), and is not used to control the passage of data between BSR cells (see, e.g., FIG. 8 and column 8:23-26).

In view of the above, the cited security circuit 650-A(1)thus functions to block test data signals 'during INTEST or other Boundary Scan procedures' as described at column 8:32-36, and does so in response to a stored security code. The '124 reference's approach to controlling or blocking the passage of test data signals is done independently of any update signal (i.e., the data is either passed or blocked entirely), and independently from any bit pattern passed between the BSR cells. The cited '124 reference thus fails to correspond to the claimed 'dedicated control circuitry' that is 'responsive to the bit pattern' captured by a second register, and thus cannot operate in accordance with the claimed dedicated control circuitry for controlling an update signal in response to a bit pattern."

Answer: the reference '124 discloses:

"FIG. 8 is a block diagram showing an IOB 800 in accordance with another embodiment of the present invention. IOB 800 is typically formed on a host PLD (not shown) and controls

an I/O pin 810 of the host PLD. IOB 800 includes three BSR cells 601(1), 601(2) and 601(3) that are connected to a core logic circuit (not shown) of the host PLD, and are linked by conductive segments that form a portion of a BSR chain of the host PLD. In addition, IOB 800 includes three security circuits 650-A(1), 650-A(2) and 650-A(3) that are connected to the BSR chain. Each of the BSR cells 601(1), 601(2) and 601(3) and security circuits 650-A(1), 650-A(2) and 650-A(3) includes the components discussed above with reference to FIG. 6(A).

(13) IOB 800 is arranged such that one security circuit is located on the BSR chain between adjacent pairs of BSR cells. BSR cell 601(1) receives TDI signals from a previous IOB (not shown) connected to the BSR chain and a DATA IN signal from input buffer IB, and outputs a SYSTEM INPUT signal that is transmitted to, for example, the core logic circuit of the host PLD. In addition, test data signals stored in shift register flip-flop 620(1) of BSR cell 601(1) are applied to a first conductive segment 625(1) of the BSR chain. Security circuit 650-A(1) is connected between first conductive segment 625(1) and a second conductive segment 675(1), which is connected to an input terminal of an input MUX 610(2) of BSR cell 601(2). BSR cell 601(2) receives data signals from BSR cell 601(1) via second conductive segment 675(1), and from a SYSTEM OUTPUT terminal that is connected to the core logic circuit. BSR cell 601(2) generates a DATA OUT signal that is transmitted to tri-state buffer TS. In addition, test data signals stored in shift register flip-flop 620(2) of BSR cell 601(2) are applied to a third conductive segment 625(2) of the BSR chain. Security circuit 650-A(2) is connected between third conductive segment 625(2) and a fourth conductive segment 675(2), which is connected to an input terminal of an input MUX 610(3) of BSR cell 601(3). BSR cell 601(3) receives data signals from BSR cell 601(2) via fourth conductive segment 675(2), and from a SYSTEM LOGIC OUTPUT ENABLE terminal connected to the core logic circuit, and generates an output enable (OE) signal that is transmitted to tri-state buffer TS. Tri-state buffer TS is controlled in response to the OE signal to transmit the DATA OUT signals to I/O pin 810.

(14) Similar to conventional IOB 116 (discussed above), IOB 800 is configured during normal operation by output enable (OE) signal (which is transmitted through BSR cell 601(3)) either to receive input data signals applied to I/O pin 810, or to transmit output data signals to I/O pin 810. When the OE signal is in a first state (e.g., low), IOB 800 is configured for receiving input signals from I/O pin 810 (i.e., tri-state buffer TS is set in a tri-state mode). In the input mode, input buffer IB transmits DATA IN signals applied to I/O pin 810 through BSR cell 601(1) and on a SYSTEM INPUT line to, for example, the core logic circuit of the host PLD. Conversely, when the OE signal is in a second state (e.g., high), IOB 800 is configured for transmitting output signals to I/O pin 810. In the output mode, output signals transmitted on a SYSTEM OUTPUT line from, for example, the core logic circuit, are applied to I/O pin 810 through BSR cell 601(2) and tri-state buffer TS." (col. 10, lines 39-67 to col. 11, lines 1-32)

In addition, the '124 reference discloses:

"PLD 900 operates as follows. When the security bit of each security circuit 650-A(XX) is disabled, each security circuit passes the test data value received from an associated BSR cell (i.e., PLD 900 operates essentially identically to conventional PLD 500, described above). In

contrast, when the security bit of each security circuit is enabled, the high INTEST signal causes each security device to generate a low (logic "0") output signal, even if the security device receives a high (logic "1") input signal. Therefore, any sequence of test data values shifted into BSR chain 905 via the TDO terminal is blocked by the security circuits associated with each IOB. Further, any test results generated by core logic circuit 918 are blocked during subsequent shift operations. An example of a resulting data stream is illustrated in test data source 910. The sample input test data pattern 1,0,0,0,0,1,1,0,0 is selected randomly. For any such input test data pattern, the output signals generated at the TDI terminal are all logic "0". Consequently, it is not possible for a would-be pirate to determine the logic implemented in core logic circuit 918 utilizing the INTEST instruction." (col. 11, lines 51-67 to col. 12, lines 1-3)

Figure 8 illustrates the cited col. 10, lines 39-67 to col. 11, lines 1-32 above. The tri-state buffer TS is controlled in response to the OE signal to transmit the DATA OUT signals to I/O pin 810 or to DATA IN via IB to the SHIFT DR 610(1) and CLOCK DR 620(1) and UPDATE 630(1) DR and up to SECURITY CIRCUIT 650-A1 via segment 625(1) and so on to make a close-loop control.

Thus, the '124 reference does teach providing correspondence to claim limitations directed to blocking an update signal for controlling the capture of a bit pattern passed between registers or to controlling an update signal as claimed.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to TOAN M. LE whose telephone number is (571)272-2276. The examiner can normally be reached on Monday through Friday from 9:00 A.M. to 5:30 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Drew Dunn can be reached on (571) 272-2312. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Toan Le
December 24, 2008

/Michael P. Nghiem/
Primary Examiner, GAU 2863